IN THE CLAIMS

The following are Claims 1-30.

1. (Original) A clock generator comprising:

a first circuit adapted to programmably receive an input signal, having a possible range of voltage levels and signal types, and modify a frequency of the input signal by a first programmable amount to generate a first input signal;

a feedback loop circuit adapted to receive a feedback signal and modify a frequency of the feedback signal by a second programmable amount to generate a second input signal;

a phase-locked loop circuit adapted to receive the first input signal and the second input signal and provide a first output signal; and

a second circuit adapted to receive the first output signal and modify a frequency of the first output signal to generate a plurality of second output signals having programmable frequencies, wherein the first and second programmable amount and the programmable frequencies are determined by data stored in electrically erasable memory.

2. (Original) The clock generator of Claim 1, further comprising input/output boundary scan circuits adapted to provide JTAG test support for the clock generator.

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3. (Original) The clock generator of Claim 2, wherein the JTAG test support provides IEEE 1149.1 compliance.

4. (Original) The clock generator of Claim 1, wherein the clock generator is in-system programmable.

5. (Original) The clock generator of Claim 4, wherein the clock generator is in-system programmable by supporting IEEE 1532 standards.

6. (Original) The clock generator of Claim 1, wherein the feedback signal is selected from an internal feedback signal and an external feedback signal.

7. (Original) The clock generator of Claim 1, wherein the phase-locked loop circuit generates a lock signal when the first input signal and the second input signal are frequency and phase locked.

8. (Original) The clock generator of Claim 1, wherein the first circuit comprises three buffers adapted to programmably accept single and differential signals.

9. (Original) The clock generator of Claim 1, wherein the signal types comprise single-ended signals and differential signals.

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10. (Original) The clock generator of Claim 1, further comprising a plurality of output circuits adapted to receive

the plurality of second output signals and programmably provide a plurality of third output signals having a range of selectable voltage levels, signal types, and output impedance.

11. (Original) The clock generator of Claim 10, wherein the output circuits are adapted to provide a flexible output banking structure.

12. (Original) The clock generator of Claim 1, further comprising a plurality of multiplexers that are controlled to select from the electrically erasable memory, which determines the frequency of the first input signal, the second input signal, and the second output signals.

13. (Original) An integrated circuit comprising:

means for selecting from a plurality of input signals and generating a first input signal having a programmable frequency;

means for selecting from a plurality of feedback signals and generating a second input signal having a programmable frequency;

a phase-locked loop adapted to receive the first input signal and the second input signal and generate a first output signal;

means for receiving the first output signal and generating second output signals having programmable frequencies;

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means for selecting from the second output signals and providing output signals each having a programmable voltage level, signal type, and output impedance; and

means for providing configurability and in-system programmability.

14. (Original) The integrated circuit of Claim 13, further comprising means for testing the integrated circuit to provide IEEE 1149.1 compliance.

15. (Original) The integrated circuit of Claim 13, further comprising means for selecting the programmable frequency for the first input signal and the second input signal and the programmable frequencies for the second output signals.

16. (Original) The integrated circuit of Claim 13, wherein the signal type comprises single-ended signals and differential signals.

17. (Original) A method of generating clock signals, the method comprising:

receiving an input signal, wherein the input signal may be a single-ended signal type or a differential signal type;

modifying a frequency of the input signal by an amount determined from data selected from memory to provide a first input signal;

receiving a feedback signal;

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modifying a frequency of the feedback signal by an amount determined from data selected from memory to provide a second input signal;

aligning a frequency and/or a phase of the first input signal and the second input signal to provide a first output signal;

modifying a frequency of the first output signal to generate a plurality of second output signals having frequencies determined from data selected from memory; and

providing output signals, selected from the second output signals, which have programmable voltage levels, signal types, and output impedances.

18. (Original) The method of Claim 17, further comprising providing configuration data to the memory.

19. (Original) The method of Claim 17, further comprising providing in-system programmability to modify configuration data stored in the memory.

20. (Original) The method of Claim 17, further comprising providing JTAG compliant functional testing.

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21. (Original) A clock generator comprising:

an input circuit programmable to receive input signals of various signal types and voltage levels and to generate in response an input signal to a phase-locked loop (PLL);

a phase-locked loop adapted to receive the PLL input signal and to generate in response a PLL output signal; and

an output circuit adapted to receive the PLL output signal and be programmable to generate in response clock signals of various signal types and voltage levels.

22. (Original) The clock generator of Claim 21, further including a clock divider circuit coupled between the input circuit and the phase-locked loop and programmable to modify a frequency of the PLL input signal.

23. (Original) The clock generator of Claim 21, further including a clock divider circuit coupled between the phase-locked loop and the output circuit and programmable to modify a frequency of the PLL output signal.

24. (Original) The clock generator of Claim 21, further including a feedback loop circuit programmable to modify a frequency of a feedback signal and to provide the modified signal as a second PLL input signal.

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25. (Original) The clock generator of Claim 21, further comprising input/output boundary scan circuits adapted to provide JTAG test support.

26. (Original) A method of generating a clock signal, the method comprising:

programmably receiving input signals of various signal types and voltage levels and generating an input signal for a phase-locked loop (PLL);

receiving the PLL input signal and generating in response a PLL output signal; and

receiving the PLL output signal and programmably generating in response clock signals of various signal types and voltage levels.

27. Original) The method of Claim 26, further comprising programmably modifying a frequency of the PLL input signal.

28. (Original) The method of Claim 26, further comprising programmably modifying a frequency of the PLL output signal.

29. Original) The method of Claim 26, further comprising programmably modifying a frequency of a feedback signal and providing the modified signal as a second PLL input signal.

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30. (Original) The method of Claim 26, further comprising providing JTAG support and IEEE 1532 in-system programmable standards.

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